REMARKS

In response to the Office Action mailed April 6, 2006, Applicants respectfully request reconsideration.

Claims 1-30 were previously pending in this application. By this amendment, Applicants amend claims 1, 10, 13, 19, 23, 25 and 26 solely for clarification. As a result, claims 1-30 are pending for examination, of which claims 1, 24, 26, and 30 are independent. No new matter has been added.

Applicants' lack of response to any of the contentions set forth in the Office Action should not be construed as Applicants' acquiescence to any such contentions, as Applicants only respond to contentions to the extent Applicants believe is necessary to place all of the claims in condition for allowance.

1.   Discussion of Background and Some Aspects of Applicants' Invention

For illustrative purposes only, Applicants provide the following discussion of the background and some aspects of Applicants' invention, which is not intended to limit the scope of the claims. The Examiner is respectfully requested to give careful consideration to the language of each of the independent claims and to address each on its own merits, without relying on this discussion. In this respect, Applicants do not rely on this example to distinguish any of the independent claims of the present invention over the asserted references, but rather, rely upon the arguments presented below.

Aspects of the present invention deal with situations in which a central processing unit (CPU) requests data from a peripheral device. As set forth on page 1, lines 18 to 30 of the present application, there is a problem with known systems dealing with this situation, in that the peripheral device may not have the necessary data ready when requested. This results in an unpredictable and potentially indefinite delay, during which time the CPU is unable to continue with any processing.

Aspects of the present application improve the flow of data through the system, for example, by providing a first-in, first-out (FIFO) register and a stream register unit to supply data from the peripheral device to the processor (e.g. components 16 and 5 in Fig. 2). In some embodiments, the data is supplied directly to the processor without going through the main bus.

Further, the stream register 5 may mediate between the processor 2 and data arriving from the peripheral device.

Thus, in some embodiments of the invention, to address the above-described problem of unprintable and potentially indefinite delay, a stream register and/or FIFO supply a first type of data, i.e., data supply from a peripheral, directly to the processor; whereas a second type of data, i.e., data from memory, is supplied to the processor through a memory bus. That is, the stream register provides a separate data path from the peripherals to the processor then the path from the RAM to the processor via the memory bus (e.g., page 3, lines 15-16; page 3, line 30-page 4, line 3). Such aspects provide an advantage over known systems (e.g., Lewis) by preventing unnecessary usage of memory bus bandwidth and power, and improves the speeds of returning data to the CPU. (page 1, lines 29-30; page 5, lines 29-30).

2.   Claims 1-23 Patentably Distinguish Over Lewis

Claim 1 stands rejected under §102(b) as purportedly being anticipated by U.S. Patent No. 6,434,649 (Lewis). Applicants respectfully traverse this rejection.

Lewis is directed to a multi-threaded, bus-mastering, input/output (I/O) channel controller architecture applicable to general purpose personal computers, computer workstations, and embedded communications in network data routing and conversion functions. (col. 1, lines 30-35).

Lewis describes an input/output (I/O) channel controller core 26 for controlling the flow of data between a number of peripherals 38, 40, 42 and a PCI bus 20. (Fig. 1b). This I/O channel controller core 26 comprises an interface module 150 for interfacing with the peripherals, an intermediate pool of "First-In, First-Out" (FIFO) buffers 172 and an interface module 148 for interfacing with the PCI bus 20. (Fig. 5A; col. 14, lines 17-43). Lewis indicates that all data arriving from the peripherals are transferred to the main random access memory (RAM) 14, 54, and the processor 12 must then access the data from the RAM 14, 54. This is clearly indicated in Fig. 3 of Lewis, which provides an exhaustive data flow diagram describing the operation of the I/O channel controller 26.

In contrast to Lewis, claim 1 recites:

> A processing system for accessing data, the processing system comprising:
> a processor for executing instructions;

> a stream register unit connected to supply *a first type* of data to the processor, the first type of data being data supplied from a peripheral;
>
> a FIFO connected to receive said first type of data from the peripheral and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the stream register unit; and
>
> a memory bus connected between a data memory and the processor, across which the processor can access *a second type* of data, the second type of data being randomly accessible data held in the data memory.

Lewis does not teach or suggest that two separate types of data can be supplied to a processor, a first type of data being data supplied from a peripheral and a second type of data being randomly accessible data held in a data memory, as required by claim 1. Rather, all data arriving from the peripherals of Lewis is transferred to the main RAM 14, 54, and the processor 12 must then access that data separately from that RAM 14, 54. Thus, although Lewis does teach generally first and second types of data as defined in independent claim 1, it does not teach that the first type of data is supplied to the processor. Instead, according to Lewis, data from the peripherals is always first transmitted to the RAM 14, 54 where it becomes the second type of data, and thus only the second type of data is supplied to the processor of Lewis.

Thus, Lewis fails to provide an advantage provided by claim 1 of preventing unnecessary usage of memory bus bandwidth and power, and improving the speed of returning data to the CPU.

In view of the foregoing, Applicants respectfully request that the rejection of claim 1 under §102(b) be withdrawn. Claims 2-23 each depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicants request that the rejections of these claims under §102(b) be withdrawn.

3.   Claims 24 and 25 Patentably Distinguish Over Lewis

Claim 24 stands rejected under §102(b) as purportedly being anticipated by Lewis. Applicants respectfully traverse this rejection.

Claim 24 recites:

> A streaming data handling system, comprising:
> a processor;
> a stream register associated with the processor;
> a FIFO memory connected to the processor via the stream register,

> **wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order.**

Lewis fails to teach or suggest the streaming data handling system recited in claim 24, in particular the limitation of "wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order." Further, it would make no sense for Lewis to operate in this manner. As noted above, the peripheral data in Lewis is always stored in the RAM 14, 54 before being accessed by the processor. Consequently, neither FIFO pool 172 nor the interface module 148 (or indeed any other component of the I/O core 26) operates a protocol which ensures that data is supplied to the processor in the received order.

In view of the foregoing, claim 24 patentably distinguishes over Lewis. Accordingly, Applicants respectfully request that the rejection of claim 24 under §102(b) be withdrawn. Claim 25 depends from claim 24 and is patentable for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claim 25 be withdrawn.

4.   Claims 26-29 Patentably Distinguish Over Lewis in view of Garcia

Claim 26 stands rejected under §103(a) as purportedly being unpatentable over Lewis in view of U.S. Patent No. 6,433,785 (Garcia). Applicants respectfully traverse this rejection.

Claim 26 recites:

A stream register connectable between a processor and a peripheral, the stream register comprising:
     a receiver arranged to receive a request for a data item from the processor; and
     a stream engine, arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor, and **if the data item is not available, send a timeout signal to the processor.**

The Office Action concedes that the feature of sending either a stall signal (claim 30) or a timeout signal (claim 26) to a processor if a data item is not available from the peripheral is not taught

by Lewis, but contends that it would be obvious to introduce from Garcia. Applicants respectfully disagree.

Firstly, because Lewis teaches transferring data from the peripherals to the memory 14, 54, rather than to the processor, at the time of the invention a person of ordinary skill in the art would have seen no reason to provide a timeout signal from the I/O core 26 to the processor of Lewis.

Secondly, Lewis explicitly teaches that after the host processor 12 initialises the I/O channel controller 23, 62, then "thereafter the host processor 12 does not participate in the actual transfer of the data stream 64 to the I/O channel controller core 62". Thus, Lewis explicitly teaches that the processor should not be involved in the transfer of data from the peripherals, but instead that that task should be left exclusively to the I/O channel controller core 23, 62. Indeed, that is the whole point of Lewis: to remove the processor from the data transfer process. Thus, to introduce the timeout counter from Garcia into Lewis would defeat the whole point of Lewis, and a person of ordinary skill in the art would not contradict the explicit teachings of Lewis in order to do so.

The Office Action contends that it would be obvious to a person of ordinary skill in the art to combine Lewis and Garcia in order to "optimise a request process in which resources are valuable and delays need to be minimised improving the processor to device throughput". Applicants respectfully disagree. There is no such alleged teaching in either of Lewis or Garcia. As the Office Action acknowledges, Lewis is completely silent on the topic of timeout signals. Further, Garcia is not in any way concerned with optimising the request for data from a peripheral device to a processor, but is instead concerned with data going in the opposite direction, i.e. being written from a processor to a graphics device 140.

For at least the foregoing reasons, the combination of Lewis and Garcia is improper, and the Office Action has failed to establish a *prima facie* case of obviousness.

Further, even if the combination were proper (which it is not), claim 26 would distinguish over such combination.

Claim 26 clearly recites sending a timeout signal to the processor if a data item is not <u>available from a peripheral</u>. In direct contrast, the timeout counter of Garcia is used to indicate that a <u>write buffer in a memory controller 120</u> is not available when processor 110 is attempting to write information to a graphics device 140. That is, the timeout counter in Garcia is <u>not</u> used to indicate whether data is available from the graphics device 140, or indeed any other peripheral. (col. 2, line 55- col. 3, line 7;

Fig. 2). Thus, even if Lewis and Garcia were combined, the resulting system would not recite a stream engine arranged to send a time-out signal to a processor if the data item is not available, as required by claim 23

In view of the foregoing, claim 26 patentably distinguishes over the combination of Lewis and Garcia. Accordingly, Applicants respectfully request that the rejection of claim 26 under §103(a) be withdrawn. Claims 27-29 each depend from claim 26 and are patentable for at least for the same reasons. Accordingly, Applicants respectfully request that the rejections of these claims under §102(b) be withdrawn.

5.   Claim 30 Patentably Distinguishes Over Lewis in View of Garcia

Claim 30 stands rejected under §103(a) as purportedly being unpatentable over Lewis in view of Garcia. Applicants respectfully traverse this rejection.

Claim 30 recites:

> A stream register connectable between a processor and a memory, the stream register comprising:
> a receiver arranged to receive a request for a data item from the processor; and
> a stream engine, arranged to send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, if the data item is available, send the data item to the processor and **if the data item is not available, send a stall signal to the processor.**

For reasons set forth above in Section 5, the combination of Lewis and Garcia is improper. Further, even if the combination were proper (which it is not), claim 30 patentably distinguishes over such combination.

For reasons that should be clear from the discussion of Lewis and Garcia set forth above, no combination of these references would include all the limitations of the stream register recited in claim 30, in particular, a receiver arranged to send a stall signal to a processor if a data item is not available.

In view of the foregoing, claim 30 patentably distinguishes over the combination of Lewis and Garcia. Accordingly, Applicants respectfully request that the rejection of claim 30 under §103(a) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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